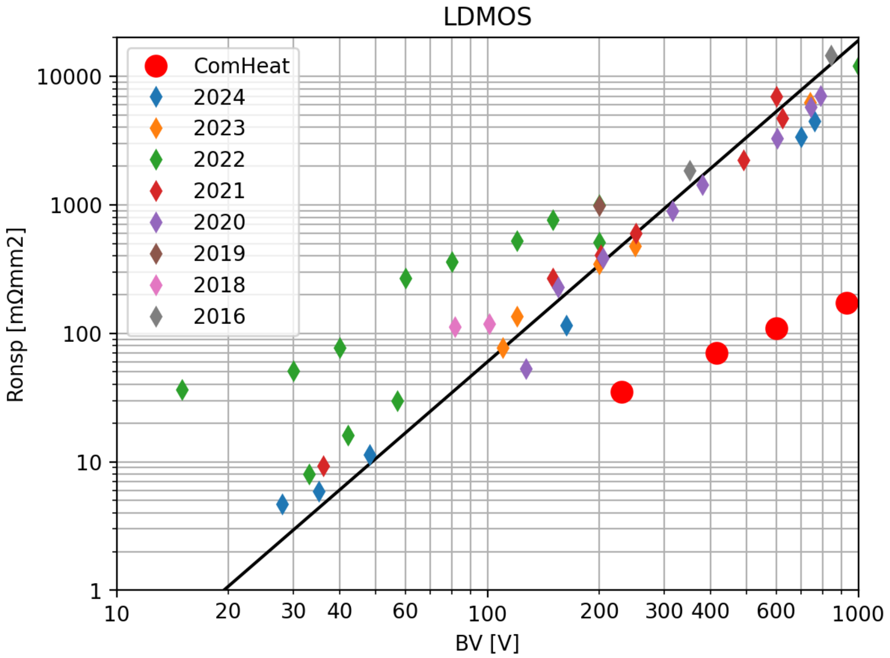
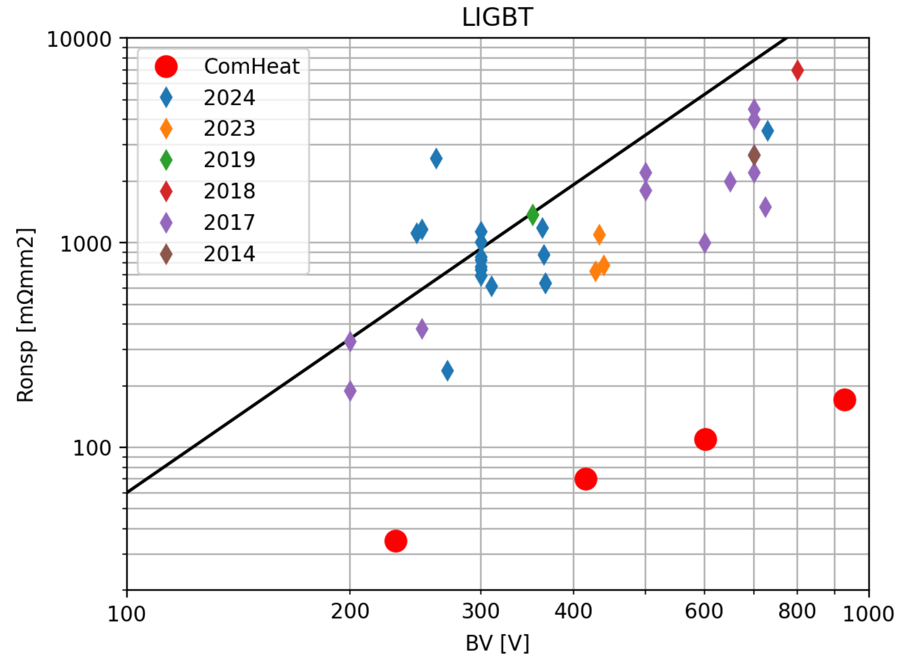
ComHeat-LIGBT compared with recent state-of-the-art LDMOS/LIGBT devices

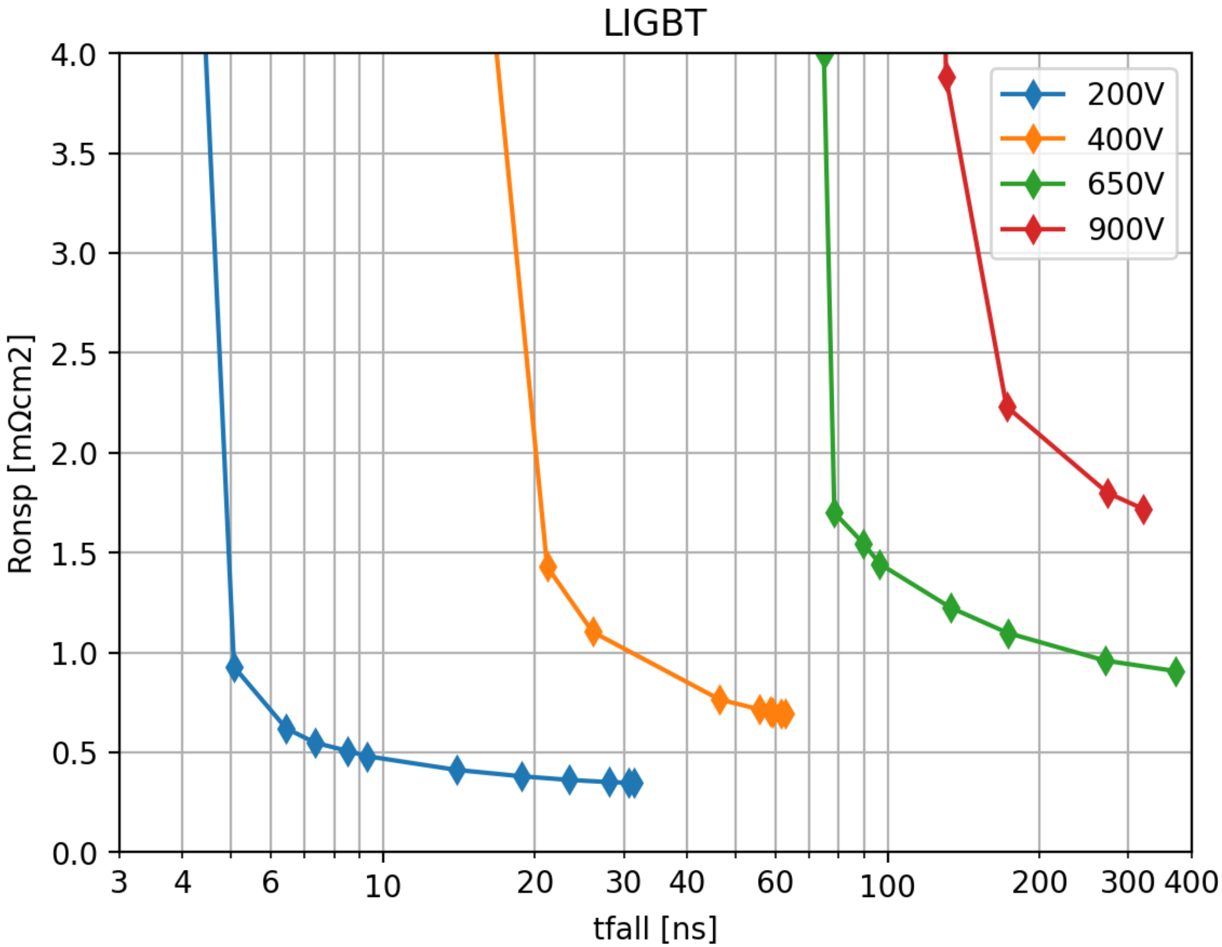




The ComHeat LIGBT has order of magnitude lower $R_{on,sp}$ than others. This gives room for increasing the $R_{on,sp}$ and thus a faster device.

$R_{on,sp}$ vs t_{fall}

- In all LIGBT's a trade-off between $R_{on,sp}$ and t_{fall} (or E_{off} and V_{on}) can be made. So in this device, as illustrated below for different voltages.



ComHeat LIGBT concept

ComHeat offers a latch-free LIGBT with superior $R_{on,sp}$ (= low cost) which can be implemented in existing technologies.

What is different to existing LIGBT technologies?

1. Much more device/area => low cost.
2. Totally immune against latch-up.

Data sheet

Voltage class	200V	400V	600V	900V
BV [V]	230	410	590	930
$R_{on,sp}$ [mΩcm^2]	0.35	0.70	1.0	1.7
t_{fall} [ns]	28	62	270	320

- The usual LIGBT t_{fall}-$R_{on,sp}$ trade-off applies (see next page). Below is what happens if t_{fall} is improved.

Voltage class	200V	400V	600V	900V
BV [V]	240	470	610	940
$R_{on,sp}$ [mΩcm^2]	0.62	1.1	1.5	2.2
t_{fall} [ns]	6.5	26	90	170
t_{fall} conditions:	I_C=6.7 A/mm V_{CC}=150V	I_C=4.5 A/mm V_{CC}=300V	I_C=3.2 A/mm V_{CC}=400V	I_C=2.4 A/mm V_{CC}=600V

- $R_{on,sp}$ conditions: V_G=5V, V_C=5V

Concept status

- The concept can be implemented in any existing BCD foundry process using standard process steps.
- To full exploit the benefits of the concept a few extra process steps (mask+implant) might be needed.
- The concept is independent of voltage class but a realistic guess is that the real gain in performance is achieved at 200-700V.
- Presented data for different voltages is simulated in different technologies incl. both SOI and bulk.
  - Generally, a SOI substrate gives a faster LIGBT's than a bulk substrate. This is also verified for ComHeat LIGBT (50% reduction of t_{fall} @ 400V).

Different paths

ComHeat sees different paths to silicon depending on collaboration partners and cost and time.

1. Implement in an existing BCD foundry technology.
   - Pros: fastest way to silicon.
   - Cons: performance might not be optimal.
2. Implement in an existing BCD process with some additional steps (2-3).
   - Pros: performance should be near optimal.
   - Cons: adding process steps adds time and cost
3. Implement in new process.
   - Pros: even better performance is possible
   - Cons: cost, time, requires backing from manufacturer to develop technology.