A New Latch-Free LIGBT on SOI

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***Abstract*— A new latch-free LIGBT on SOI is presented. The new device combines advantages from both LDMOS as well as LIGBT technologies; high breakdown voltage, high drive current density, low control voltages, at the same time eliminating latch-up problems. Breakdown voltage of over 200 V, on-state current density over 3 A/mm and latch-free operation is demonstrated.**

I. Introduction

Lateral Double-diffused MOS (LDMOS) and Lateral Insulated Gate Bipolar Transistor (LIGBT) devices are very commonly used in a wide variety of power electronic applications. The LDMOS transistor provides higher speed but lower current densities than the LIGBT device. The LIGBT on the other hand can handle extremely high current densities due to high injection (conductivity modulation) and low on-resistance. Integration of LDMOS and LIGBT on SOI substrate provides additional advantages in terms of possibility to integrate with CMOS thus realizing multi-functional high-performance Power-IC [1-3] and also more efficient RESURF. However, LIGBT devices are prone to latch-up at higher current densities already at rather low voltages.

The LIGBT is essentially a combination of a bipolar transistor (BJT) and a MOSFET, see Fig. 1. The BJT provides the high current capability and the off-state voltage handling capability, while the MOSFET provides a high-impedance voltage control of the bipolar base current.

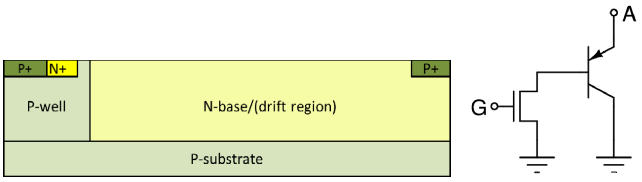

Figure 1. Schematic of an LIGBT consisting of and NMOS and a p-n-p BJT and a corresponding equivalent circuit.

The LIGBT can be implemented both in junction-isolated bulk technology and in SOI technology. Major challenges are to achieve a low on-voltage V_{ON} (low on-state losses), while controlling the electric field to have a high breakdown voltage, and at the same time reduce the latch-up behavior. In bulk technology, traditional RESRUF [4] works quite well for the off-state design of the drift region, but does not necessarily result in a good on-state performance. A good overview of different schemes to implement LIGBT is given in [5].

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The latch-up phenomenon that takes place in an LIGBT is due to the parasitic bipolar n-p-n transistor, i.e. carriers injected into the collector triggering the source of the MOSFET (the parasitic n+ emitter) to inject more carriers into the base of the p-n-p, thereby the gate loses control of the p-n-p base current. Numerous attempts have been made to solve this problem, but none fully solving it without trade-off in the performance.

Here, a new SOI-LIGBT concept is presented where the region sensitive for triggering the latch-up is separated from the p-n-p bipolar part of the transistor, thus totally eliminating the latch-up. It is schematically shown in Fig. 2. The drain of the MOSFET is connected to the base of the p-n-p BJT, thus providing and controlling the electron base current. The hole current injected from the anode is collected in the p-n-p structure and does therefore not have the possibility to trigger electron injection from the MOSFET.

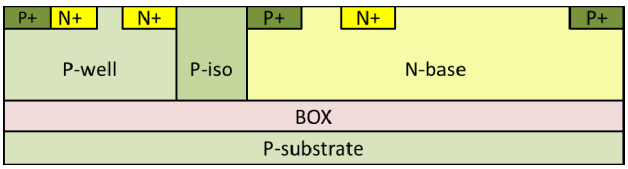

Figure 2. The new LIGBT concept where the MOSFET is separated from the BJT-part of the device, thus effectively eliminating the latch-up behavior.

The separation of the MOSFET and the BJT also opens up for additional freedom in designing the device. In fact, a low voltage sub-micron MOSFET with very high-current drive capability can be used to deliver the base current of the LIGBT, provided its drain potential is kept low during all regions of operation. Furthermore, the effective width of the BJT and the MOSFET can separately be tuned to the desired device performance [6].

II. Device Design and Operation Principle

The new LIGBT concept is here implemented in a high-voltage SOI process featuring a 1 µm thick BOX, deep-trench isolation (DTI) and a partial SOI solution offering the possibility to locally set a high voltage in the substrate. The process also offers a lateral super-junction (SJ), with doping levels optimized for breakdown voltages over 200 V. The lateral SJ is similar to RESURF concepts that successfully have been used previously in LDMOS [7, 8]. The MOSFET part

(the controlling device) is in this LIGBT implementation realized by an LDMOS with typical breakdown of >12 V. The p-n-p bipolar part is separated from the LDMOS using DTI and is designed using the lateral SJ, which acts as the base region. Deep wells define the collector region and the n-buffer region on the anode (emitter) side, respectively. A schematic cross-section of the implemented LIGBT device is shown in Fig. 3.

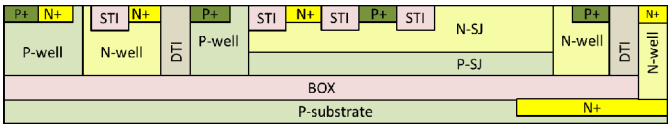

Figure 3. Schematic cross-section of the LIGBT. The drain of the LDMOS controls the electron base current to the p-n-p bipolar part. The p+ anode has an n-buffer using the n-well. An opening in the BOX connects a buried n-layer to high voltage (200 V)

The SJ-region determines the off-state breakdown voltage. Using the partial-SOI solution a buried n-layer under the BOX is connected to the front, where it is set to high-voltage (200 V) during operation. A detailed analysis of the off-state design of a SJ in partial SOI technology is given in [9]. Careful design of the p-n-p part, involving field plates (not shown in Fig. 3) and a p-shield, ensures that in the off-state, the region close to the n+ base-contact is depleted thus protecting the thin gate oxide of the LDMOS transistor. Effective depletion of the base already at very low voltages prevents the p+ anode to become sufficiently forward biased to start inject holes. Basically, the structure behaves as an open-base p-n-p in off-state. At high anode voltage the 1 µm BOX will normally limit the breakdown. However, by setting the buried n-layer to a high potential the electric field at the high-side will be drastically reduced and the off-state breakdown voltage is mainly determined by the lateral SJ base region.

In the on-state the gate opens a channel and connects to the n-base region. As the anode voltage increases it becomes forward-biased and holes are injected into the SJ base region, to be collected by the p-well/p+ collector. At sufficiently high forward anode voltage high injection occurs and the resistance of the base drastically gets reduced, thus resulting in a very low total forward voltage drop (V_{ON}) of the LIGBT. Charge-balance needs to be fulfilled, consequently at high injection, electrons are supplied from the LDMOS, and thus the gate controls the total anode current. As the anode voltage is further increased a potential drop is starting to build-up in the base region. A proper design will allow the base contact to rise to a potential well below the breakdown of the LDMOS but at the same time sufficiently high to be well into saturation region of the LDMOS I-V characteristic, i.e. also the anode current enters saturation. Hereafter, the base potential should not increase significantly in order to avoid premature on-state breakdown.

A test chip consisting of several variations of the new LIGBT, as well as other test structures, was designed and manufactured at foundry. A chip photo is shown in Fig. 4. LIGBT structures were manufactured that allow separate characterization of both the LDMOS and the p-n-p device.

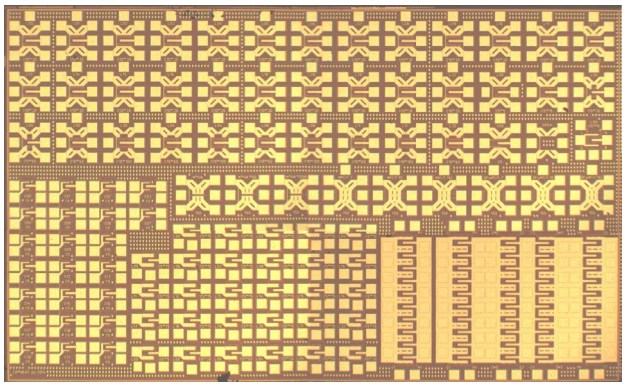

Figure 4. Manufactured chip 2.5x4 mm^2.

III. Results and Discussion

Measurements were carried out on LIGBTs having a probe configuration, see Fig. 5, suitable for RF- and DC-measurements. An additional pad was used to connect to the buried n-layer. This contact was kept at high voltage (200 V) for all measurements. DC-measurements were performed using a HP-4142B parameter analyzer and analog curve-tracers. High-frequency measurements were carried out using a network vector analyzer (NVA), from which cut-off frequencies and terminal capacitances were extracted.

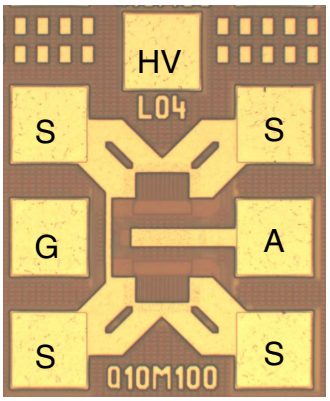

Figure 5. LIGBT with RF-pad configuration. A: anode, G: gate, S:source and collector, and HV: high-voltage buried n-layer.

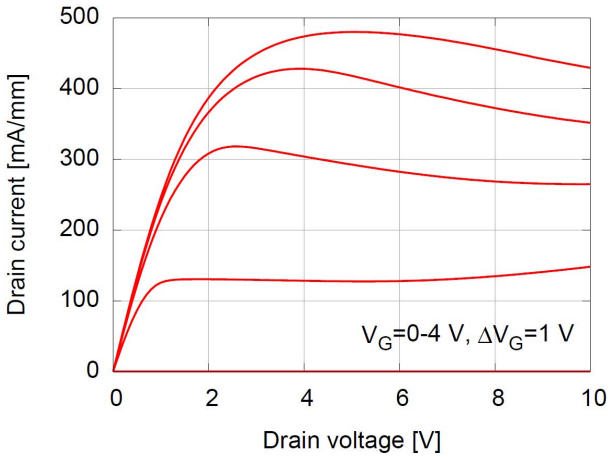

Figure 6. I-V characteristics of the LDMOS transistor that controls the LIGBT base current.

An important part of the LIGBT is the LDMOS transistor that controls the base current. The I-V characteristics of the LDMOS measured separately is shown in Fig. 6. Quite severe self-heating is observed due to the BOX [10]. The measured threshold voltage is 0.5 V and the breakdown voltage is 12 V.

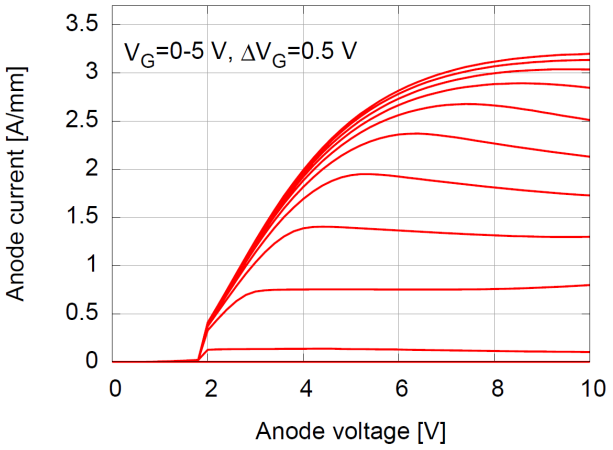

Figure 7. I-V characteristics of the LIGBT showing the anode current per width of the p-n-p. Gate width of LDMOS is 6x the width of the p-n-p part.

The full LIGBT device has an off-state breakdown voltage of around 220 V, verifying that the lateral-SJ and the buried high-voltage n-layers are properly designed. Different combination of widths for the LDMOS and the p-n-p part were manufactured and characterized. Figure 7 shows the measured I-V characteristics for and LIGBT device where the width of the LDMOS is 6x the p-n-p part. Latch-free operation is observed and characteristics that saturates due to the LDMOS control of the base current. The device demonstrates extremely high saturation current densities, over 3 A/mm, with respect to p-n-p width. This is more than an order higher than what has been reported for similar SJ LIGBTs on SOI [3, 11], and obviously much more than an order higher than state-of-the-art 200 V LDMOS devices. This is an extremely high current density for any silicon device. The high injection kicks-in at an anode voltage of approximately 2 V. The compression at higher gate voltages is due to the compression in the LDMOS characteristics, see Fig. 6.

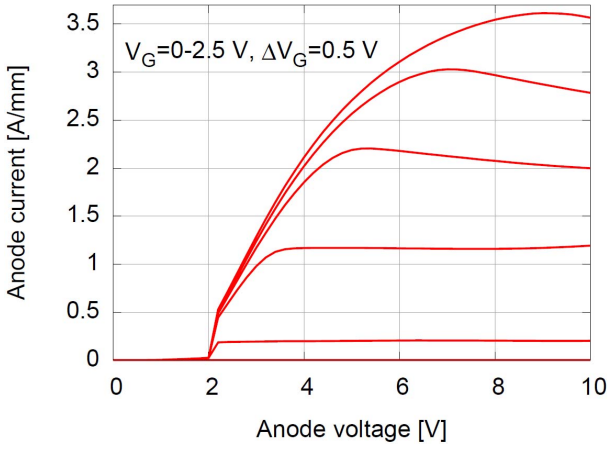

Figure 8. I-V characteristics of the LIGBT showing the anode current per width of the p-n-p. Gate width of LDMOS is 10x the width of the p-n-p part.

Keeping the p-n-p width but increasing the LDMOS gate width to 10x of the p-n-p width increases the anode current further. In fact, it scales very well with the LDMOS width, indicating that the base of the p-n-p indeed has a very low resistance and does not limit the current. Figure 8 shows the increased current for a scaled device. It is worth pointing out a significant advantage of this new concept; that not only the saturation current can be scaled, but also the on-resistance is significantly reduced. This means that either for a given on-state voltage drop the current can be scaled using just a scaled gate width, or for a given current density the on-state voltage drop can be tuned by the gate width, i.e. the on-resistance is almost independent on the size of the p-n-p device. The effective on-resistance for the LIGBT device in Fig. 7 is around 2 Ωmm and consequently less for the device in Fig. 8 where the LDMOS width is larger.

It is also worth emphasizing that the extremely high current densities are not a result of some current amplification effect. Figure 9 shows a measurement of only the p-n-p bipolar transistor part of the LIGBT, plotting the emitter (anode) current as a function of emitter voltage and base current. As can be seen it is a very well behaved bipolar transistor with almost ideal characteristics. However, the current gain is below unity due to the very long base. In fact the gain is only around 0.2-0.3 as seen from the characteristics. The characteristic also clearly shows the effect of the conductivity modulation of the base; a very low resistance of around 1 Ωmm is observed already for current densities much lower than demonstrated in Fig. 7 and 8.

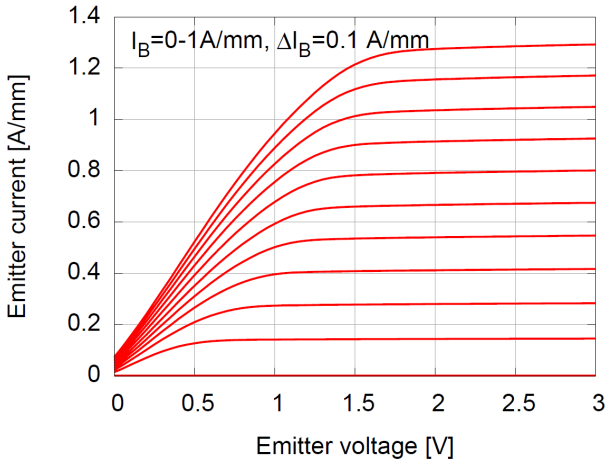

Figure 9. The bipolar characteristics of the LIGBT. Current gain is less than unity due to the long base region.

S-parameter measurements were carried out with the NVA at different frequencies, using RF-probes and a separate DC-probe for the high-voltage buried n-layer. The parasitic contribution from the RF-pad pattern was de-embedded using open-pad structures and calibration standard procedures. From the s-parameters the current-gain cut-off frequency f_T and the unit power gain cut-off frequency f_{MAX} were extracted. Figure 10 shows the f_T and f_{MAX} as a function of gate voltage for a LIGBT where the gate width of the LDMOS is 3x of the p-n-p device. The anode voltage is 10 V. The maximum f_T is 3 GHz and f_{MAX} is 5.6 GHz. Considering a breakdown of 220-230 V these cut-off frequencies are among the highest reported for

silicon devices in this range of breakdown voltage. The roll-off observed, is mainly due to the roll-off in transconductance observed in the LDMOS transistor and to some extent due to the non-linear gate capacitance.

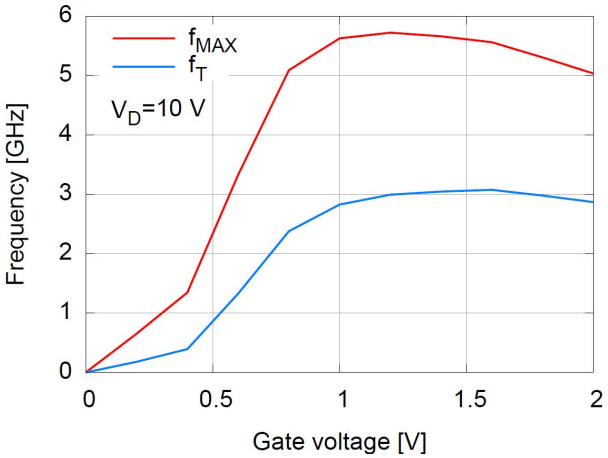

Figure 10. The measured cut-off frequencies for an anode voltage of 10 V.

Finally, off-state capacitances were extracted from the measured s-parameters at 1 GHz, see Fig. 11. The capacitive coupling between the anode and the gate (Cgd) is very low, as expected due to the separation of the LDMOS and the p-n-p device. The anode-to-ground (source and collector) capacitance is very low, in the order of 0.3 pF/mm for an almost fully depleted SJ-region. This indicates that switching performance and as well as RF-power performance can be expected to be very good. This is planned to be evaluated in the near future.

The results presented in this paper clearly demonstrated that the new LIGBT concept offer latch-free operation and astonishing performance. Furthermore, it is possible to use very low control voltage on the gate enabled by the separation and the possibility to use a very wide LDMOS. The design of the p-n-p device is very critical; effective shielding of the base to prevent LDMOS breakdown, careful RESURF of the SJ-region and the anode/n-buffer region [11] to prevent premature off-state breakdown and optimize on-state voltage drop, V_{ON}.

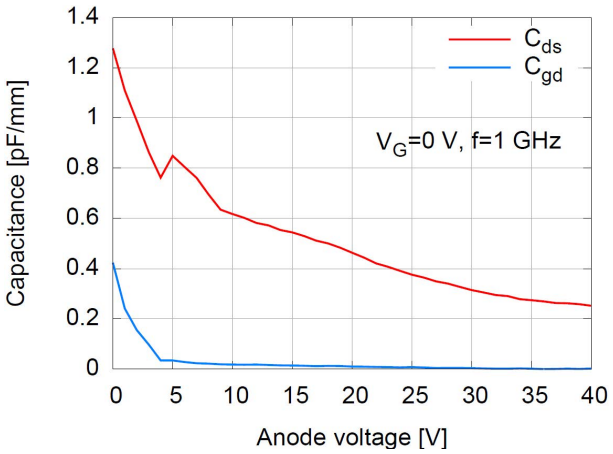

Figure 11. The off-state anode-source capacitance (Cds) and the gate-anode (Cgd) capacitance extracted from s-parameters at 1 GHz.

IV. Conclusion

A new LIGBT concept on SOI is demonstrated. By separation of the MOSFET part and the bipolar part of the device, parasitic latch-up is totally eliminated. The LIGBT is manufactures in a 1 µm BOX SOI foundry technology using a 12 V LDMOS transistor as the MOSFET part of the device. The demonstrated device has an off-state breakdown voltage higher than 200 V and extremely high current densities in excess of 3 A/mm. The device offers unique opportunities to tune and optimize the device performance by separate scaling of the different device parts.

Acknowledgment

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