Solid-State Electronics xxx (2015) xxx–xxx

Contents lists available at ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

A new latch-free LIGBT on SOI with very high current density and low drive voltage ☆

J. Olsson [a,*], L. Vestling [b], K.-H. Eklund [b]

[a] Uppsala University, The Ångström Lab/FTE, Uppsala, Sweden
[b] Comheat Microwave AB, Uppsala, Sweden

ARTICLE INFO

Article history:
Available online xxxx

ABSTRACT

A new latch-free LIGBT on SOI is presented. The new device combines advantages from both LDMOS as well as LIGBT technologies; high breakdown voltage, high drive current density, low control voltages, at the same time eliminating latch-up problems. The new LIGBT has the unique property of independent scaling of the input control device, i.e. LDMOS, and the output part of the device, i.e. the p–n–p part. This allows for additional freedom in designing and optimizing the device properties. Breakdown voltage of over 200 V, on-state current density over 3 A/mm, specific on-resistance below 190 mΩ mm^2, and latch-free operation is demonstrated.

1. Introduction

Lateral Double-diffused MOS (LDMOS) and Lateral Insulated Gate Bipolar Transistor (LIGBT) devices are very commonly used in a wide variety of power electronic applications. The LDMOS transistor provides higher speed but lower on-current densities than the LIGBT device. The LIGBT on the other hand can handle extremely high current densities due to high injection (conductivity modulation) and its low on-resistance. Integration of LDMOS and LIGBT on SOI substrate provides additional advantages in terms of possibility to integrate with CMOS thus realizing multi-functional high-performance Power-IC [1–3] and also more efficient RESURF. However, LIGBT devices are prone to latch-up at higher current densities already at rather low voltages.

The LIGBT is essentially a combination of a bipolar transistor (BJT) and a MOSFET, see Fig. 1. The BJT provides the high current capability and the off-state voltage handling capability, while the MOSFET provides a high-impedance voltage control of the bipolar base current.

The LIGBT can be implemented both in junction-isolated bulk technology and in SOI technology. Major challenges are to achieve a low on-voltage V_{ON} (low on-state losses), while controlling the electric field to have a high breakdown voltage, and at the same time reduce the latch-up behavior. In bulk technology, traditional RESURF [4] works quite well for the off-state design of the drift region, but does not necessarily result in a good on-state performance. A good overview of different schemes to implement LIGBT is given in [5].

The latch-up phenomenon that takes place in an LIGBT is due to the parasitic bipolar n–p–n transistor, i.e. carriers injected into the collector triggering the source of the MOSFET (the parasitic n + emitter) to inject more carriers into the base of the p–n–p, thereby the gate loses control of the p–n–p base current. Numerous attempts have been made, on both bulk and SOI, to reduce or solve this problem [6–10], but none fully eliminating the latching behavior.

Here, a new SOI-LIGBT concept is presented where the region sensitive for triggering the latch-up is separated from the p–n–p bipolar part of the transistor, thus totally eliminating the latch-up. The concept is schematically shown in Fig. 2. The drain of the MOSFET is connected to the base of the p–n–p BJT, thus providing and controlling the electron base current. The hole current injected from the anode is collected in the p–n–p structure and does therefore not have the possibility to trigger electron injection from the MOSFET.

The separation of the MOSFET and the BJT also opens up for additional freedom in designing the device. In fact, a low voltage sub-micron MOSFET with very high-current drive capability can be used to deliver the base current of the LIGBT, provided its drain potential is kept low during all regions of operation. This means that a very low drive voltage can control a very high total anode current. Furthermore, the effective width of the BJT and the MOSFET can separately be tuned to the desired device performance [11].

☆ The project is part of the research and development program "Innovative ICT", financed by VINNOVA (the Swedish Innovation Agency), Comheat Microwave AB and with additional support from Uppsala university.

* Corresponding author.
E-mail address: jorgen.olsson@angstrom.uu.se (J. Olsson).

http://dx.doi.org/10.1016/j.sse.2015.08.011
0038-1101/

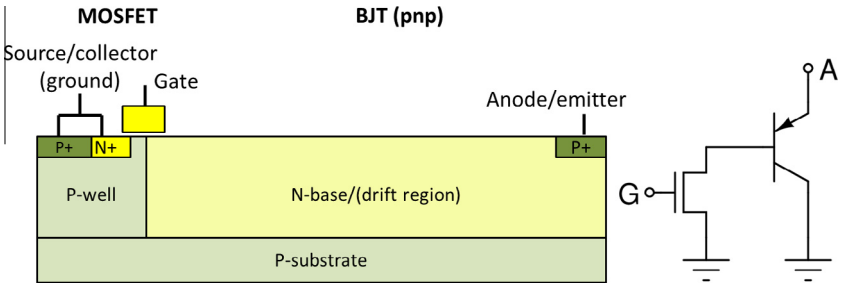

Fig. 1. Schematic of an LIGBT consisting of and NMOS and a p–n–p BJT and a corresponding equivalent circuit.

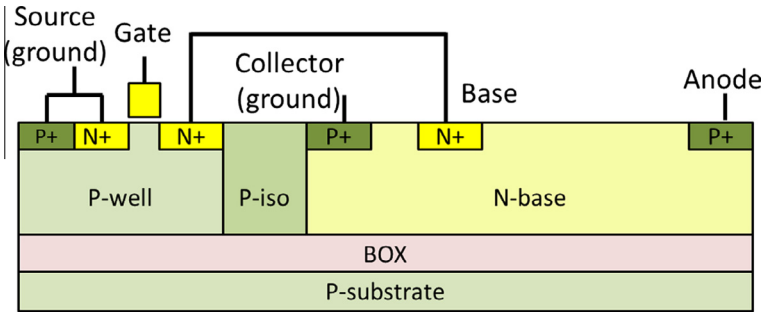

Fig. 2. The new LIGBT concept where the MOSFET is separated from the BJT-part of the device, thus effectively eliminating the latch-up behavior.

In the following, the new device concept will be presented in more detail along with its operation principle, the test chip design at foundry, results from *I–V* and *C–V* and high frequency measurements, as well as some supporting TCAD simulations to explain the operation principle.

2. Device design and operation principle

The new LIGBT concept is here implemented in a high-voltage SOI process featuring a 1 μm thick BOX, deep-trench isolation (DTI) and a partial-SOI solution offering the possibility to locally set a high voltage in the substrate through a reversed-bias diode. The process also offers a lateral super-junction (SJ), with doping levels optimized for breakdown voltages over 200 V. The lateral SJ is similar to RESURF concepts that successfully have been used previously in e.g. LDMOS transistors [12,13]. The MOSFET part (the controlling device) is in this LIGBT implementation realized by an LDMOS with typical breakdown of >12 V. The p–n–p bipolar part is separated from the LDMOS using DTI and is designed using the lateral SJ, which acts as the base region. Deep wells define the collector region and the n-buffer region on the anode (emitter) side, respectively. A schematic cross-section of the implemented LIGBT device is shown in Fig. 3.

The SJ-region determines the off-state breakdown voltage. Using the partial-SOI solution a buried n-layer under the BOX is connected to the front side, where it is set to high-voltage (200 V) during operation. The buried n-layer forms a diode to the substrate, which is reversed biased during all operation. The lowly doped p-substrate is thus depleted in the area close to the high-voltage side of the LIGBT. A detailed analysis of the off-state design of a SJ in partial SOI technology is given in [14]. Careful design of the p–n–p part, involving both poly and metal field plates (for more details se Fig. 10) and a p-shield, ensures that in the off-state, the region close to the n+ base-contact is depleted thus protecting the thin gate oxide of the LDMOS transistor. Effective depletion of the base already at very low voltages prevents the p + anode to become sufficiently forward biased to start hole injection. Basically, the structure behaves as an open-base p–n–p in off-state, since the LDMOS in off-state has its drain floating. At high anode voltage the 1 μm BOX will normally limit the breakdown. However, by setting the buried n-layer to a high potential the electric field at the high-side will be drastically reduced and the off-state breakdown voltage is mainly determined by the lateral SJ base region.

In the on-state the gate opens a channel in the LDMOS and connects to the n-base region of the p–n–p part, thus forming a p–n diode between anode and ground. As the anode voltage increases it becomes forward-biased and holes are injected into the SJ base region, to be collected by the p-well/p+ collector. At sufficiently high forward anode voltage high injection occurs and the resistance of the base drastically gets reduced, thus resulting in a very

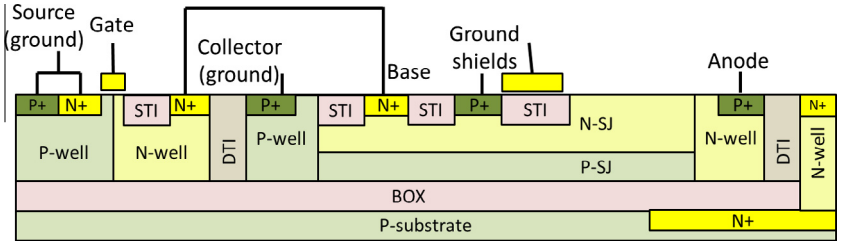

Fig. 3. Schematic cross-section of the LIGBT. The drain of the LDMOS controls the electron base current to the p–n–p bipolar part. The p + anode has an n-buffer using the n-well. An opening in the BOX connects a buried n-layer to high voltage (200 V).

Please cite this article in press as: Olsson J et al. A new latch-free LIGBT on SOI with very high current density and low drive voltage. Solid State Electron (2015), http://dx.doi.org/10.1016/j.sse.2015.08.011

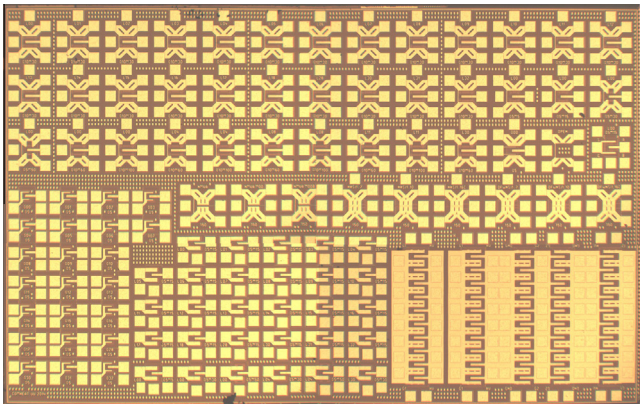

Fig. 4. Manufactured chip with the area 2.5 × 4 mm^2.

low total forward voltage drop (V_{ON}) of the LIGBT. Charge-balance needs to be fulfilled, consequently at high injection, electrons are supplied from the LDMOS, and thus the gate controls the total anode current. As the anode voltage is further increased a potential drop is starting to build-up in the base region. A proper design will allow the base contact to rise to a potential well below the breakdown of the LDMOS but at the same time sufficiently high to be well into saturation region of the LDMOS *I–V* characteristic, i.e. also the anode current enters saturation. Hereafter, the base potential should not increase significantly in order to avoid premature on-state breakdown. It should also be noted that a significant part of the hole current is carried through the p-shield, which therefore needs to be designed robustly.

A test chip consisting of several variations of the new LIGBT, as well as other test structures, was designed and manufactured at foundry. A chip photo is shown in Fig. 4. LIGBT structures were manufactured that allow separate characterization of both the LDMOS and the p–n–p device.

3. Results and discussion

Measurements were carried out on LIGBTs having a probe configuration, see Fig. 5, suitable for RF- and DC-measurements. An additional pad was used to connect to the buried n-layer. This contact was kept at high voltage (200 V) for all measurements. DC-measurements were performed using a HP-4142B parameter analyzer and analog curve-tracers. High-frequency measurements were carried out using a network vector analyzer (NVA), from which cut-off frequencies and terminal capacitances were extracted from the measured S-parameters.

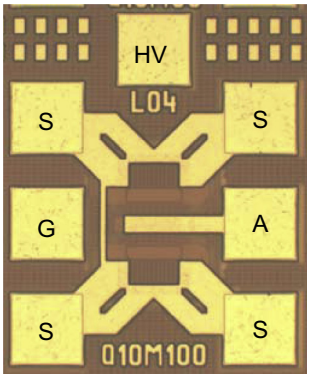

Fig. 5. LIGBT with RF-pad configuration. A: anode, G: gate, S: source, collector and p-shield, and HV: high-voltage buried n-layer.

An important part of the LIGBT is the LDMOS transistor that controls the base current. The *I–V* characteristics of the LDMOS measured separately is shown in Fig. 6. Quite severe self-heating is observed due to the BOX [15]. The measured threshold voltage is 0.5 V and the breakdown voltage is 12 V. The effective on-resistance, at V_D = 1 V and I_D = 250 mA/mm, is around 4 Ω mm.

The full LIGBT device has an off-state breakdown voltage of around 220 V, verifying that the lateral-SJ and the buried high-voltage n-layers are properly designed. Different combination of widths for the LDMOS and the p–n–p part were manufactured and characterized. Fig. 7 shows the measured *I–V* characteristics for and LIGBT device where the width of the LDMOS is 6x wider than the p–n–p part. Latch-free operation is indeed observed, even at very high current densities, and the characteristics saturate due to the LDMOS control of the base current. The device demonstrates extremely high saturation current densities, over 3 A/mm, with respect to the p–n–p width. This is more than an order higher than what has been reported for similar SJ LIGBTs on SOI [3,16], and obviously much more than an order higher than state-of-the-art 200 V LDMOS devices. This is an extremely high current density for any silicon device. The high injection kicks-in at an anode voltage of approximately 2 V. This is higher than the ideal value of around 0.7 V, and is due to voltage drop occurring in the SJ region during the turn-on process, i.e. a higher anode voltage is needed before 0.7 V develops over the injection junction at the anode side. The compression at higher gate voltages is due to the transconductance compression in the LDMOS characteristics, as seen in Fig. 6. Some-self heating is also evident, but mainly due from the LDMOS part. In fact, the LDMOS and the p–n–p part have different signs of the temperature coefficient, thus negative resistance behavior is less evident for the LIGBT. However, the device becomes very hot increasing the voltage or current further. The determination of the SOA (safe operation area) is a subject for further characterization and studies. The effective on-resistance, at I_D = 2 A/mm, is around 2 Ω mm, i.e. lower than the LDMOS above. This clearly demonstrates the advantages of the new LIGBT; lower on-resistance, much higher current densities and much higher breakdown voltages (12 V vs. 220 V) compared to the LDMOS transistor.

Keeping the p–n–p width the same but increasing the LDMOS gate width to 10x of the p–n–p width increases the anode current density further. In fact, it scales very well with the LDMOS width, indicating that the base of the p–n–p indeed has a very low resistance and does not limit the current. Fig. 8 shows the increased current for a scaled device. It is worth pointing out a significant advantage of this new concept; that not only the saturation current can be scaled, but also the on-resistance is significantly reduced.

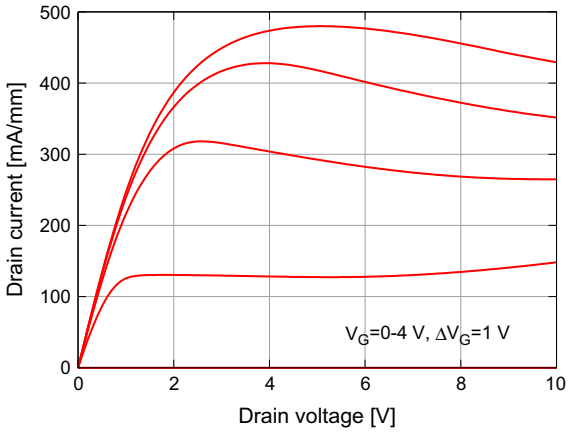

Fig. 6. *I–V* characteristics of the LDMOS transistor that controls the LIGBT base current.

Please cite this article in press as: Olsson J et al. A new latch-free LIGBT on SOI with very high current density and low drive voltage. Solid State Electron (2015), http://dx.doi.org/10.1016/j.sse.2015.08.011

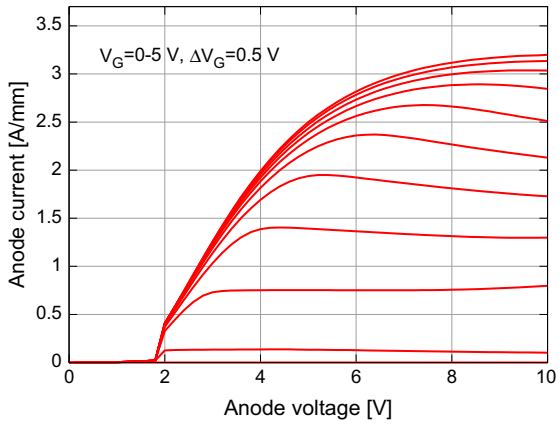

Fig. 7. *I–V* characteristics of the LIGBT showing the anode current per width of the p–n–p. Gate width of LDMOS is 6× the width of the p–n–p part.

This means that either for a given on-state voltage drop the current can be scaled using just a scaled gate width, or for a given current density the on-state voltage drop can be tuned by the gate width, i.e. the on-resistance is almost independent on the size of the p–n–p device. The effective on-resistance for the LIGBT device in Fig. 7 is around 2 Ω mm and consequently even less, around 1.8 Ω mm, for the device in Fig. 8 where the LDMOS width is larger. Note, that the gate voltage generating this current is only 2.5 V as compared to 5 V in Fig. 7. Consequently, an important advantage of scaling the LDMOS width is that a given saturation current density is obtained at a much lower gate voltage. That means that the LIGBT can be integrated with low voltage circuitry that can easily provide sufficient voltage levels to drive and control the high-voltage high-current LIGBTs.

It is also worth emphasizing that the extremely high current densities are not a result of some bipolar current amplification effect. Fig. 9 shows a measurement of only the p–n–p bipolar transistor part of the LIGBT, plotting the emitter (anode) current as a function of emitter voltage and base current. As can be seen it is a very well behaved bipolar transistor with almost ideal characteristics. However, the current gain is below unity due to the very long base. In fact the gain is only around 0.2–0.3 as seen from the characteristics. The characteristics also clearly show the effect of the conductivity modulation of the base; a very low resistance of around 1 Ω mm is observed already for current densities much lower than demonstrated in Figs. 7 and 8.

The p–n–p part is critical for the behavior of the LIGBT. In off-state the SJ is fully depleted as already mentioned. This is seen in Fig. 10, which shows results from TCAD simulation of the p–n–p part. The LDMOS is included in the simulation, but not shown here. The cross-section is similar to that in Fig. 3. The whole region is depleted and the potential is fairly well distributed along the device. A poly-silicon shield is included in the TCAD structure, as well as in the real manufactured devices, which together with the p-shield help deplete the area close to the base contact region. This is crucial in order to prevent breakdown in the LDMOS transistor, which has its drain connected to the base contact. The effect of the buried n-layer is also evident, since it forms a reverse biased p-n junction to the substrate, which consequently will deplete the substrate underneath the BOX, thereby spreading the potential lines along the BOX layer.

In on-state at high anode voltage, V_A = 160 V, see Fig. 11, this depletion effect of the substrate remains, and the potential lines are even more evenly distributed in the SJ layer. However, in on-state, the p–n–p part is under high injection condition with very high carrier concentrations. The color scale corresponds to the hole carrier concentration. It is interesting to observe that the hole concentration in the n-well region surrounding the p+ anode is very high, indicating efficient high injection and conductivity modulation of this region, while the hole concentration is some order of magnitude lower in the SJ area (however, still high injection condition). Consequently the voltage drop develops mainly in the SJ region where the effective sheet resistance is higher than in the n-well. This comes from the fact that the electron supply is limited by what is provided in electron current from the base contact, i.e. the LDMOS transistor, thus setting the limit for the high injection condition. While, in the n-well, the background electron concentration is much higher, thus allowing for a higher hole concentration within the charge neutrality boundary. Also in the on-state, the p-shield and the poly-silicon shield have important functions to protect the base contact from the high anode potential.

When the LIGBT turns on, i.e. when high injection occurs in the SJ region, the series resistance of the p–n–p parts becomes very low. The anode current then increases rapidly until the current saturates due to the LDMOS transistor that limits the supply of electrons (i.e. the LDMOS is in saturation region). It has been demonstrated in both Figs. 7 and 8 that it is possible to scale the total anode saturation current and the effective on-resistance by scaling the width of the LDMOS transistor. Increasing the LDMOS width increases current and lowers the on-resistance. However, increasing the width of the LDMOS also increases its area. Consequently, at some point the specific on-resistance is expected to

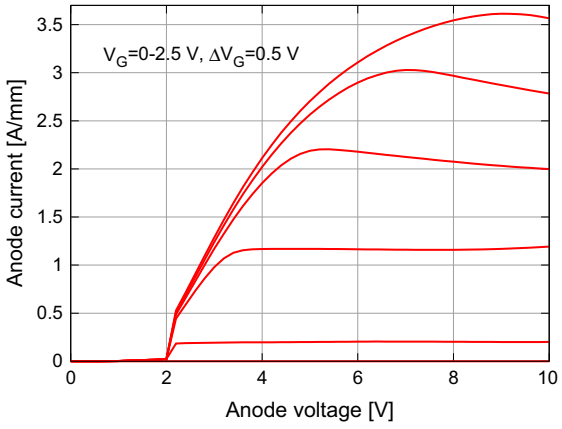

Fig. 8. *I–V* characteristics of the LIGBT showing the anode current per width of the p–n–p. Gate width of LDMOS is 10× the width of the p–n–p part.

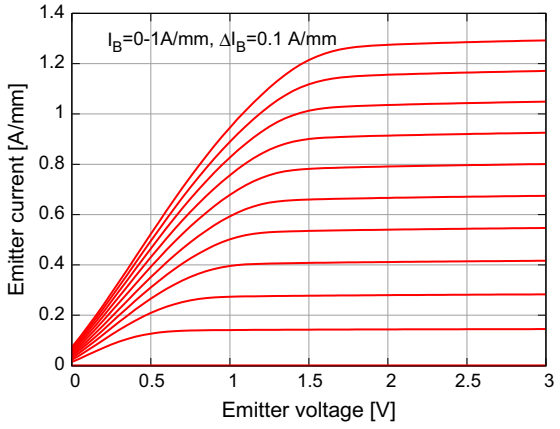

Fig. 9. The bipolar characteristics of the LIGBT. Current gain is less than unity due to the long base region.

Please cite this article in press as: Olsson J et al. A new latch-free LIGBT on SOI with very high current density and low drive voltage. Solid State Electron (2015), http://dx.doi.org/10.1016/j.sse.2015.08.011

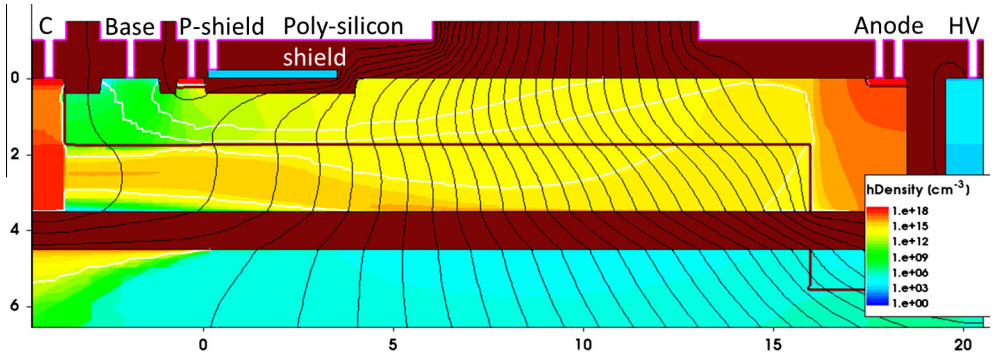

Fig. 10. TCAD simulation of the LIGBT in off-state. Cross-section of the p–n–p part showing the potential lines and the hole concentration. V_G = 0 V and V_A = 220 V.

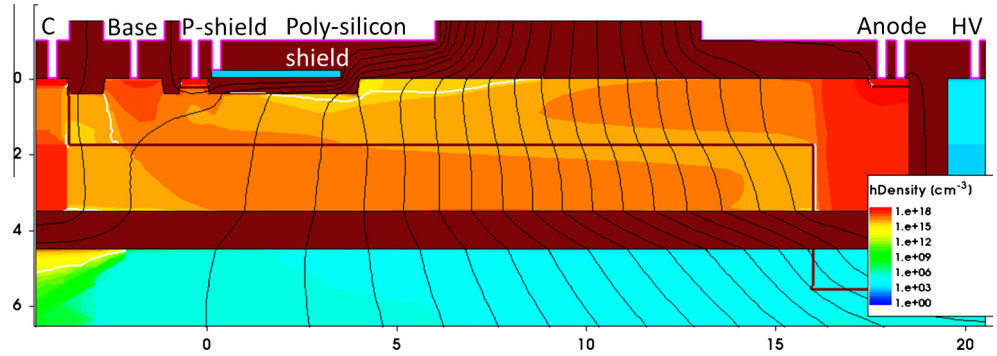

Fig. 11. TCAD simulation of the LIGBT in on-state. Cross-section of the p–n–p part showing the potential lines and the hole concentration. I_A = 1 A/mm and V_A = 160 V.

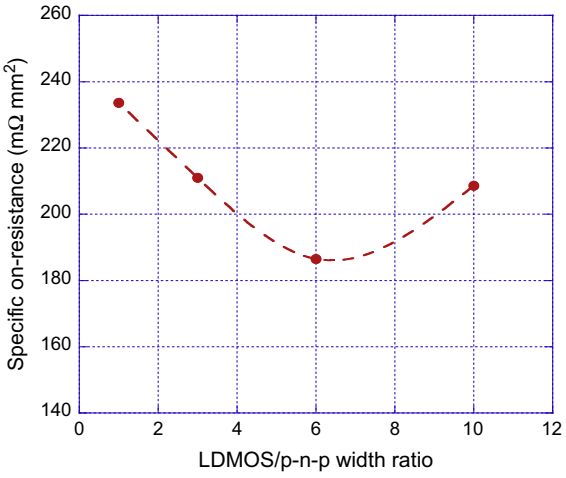

Fig. 12. LIGBT specific on-resistance as a function of the LDMOS/p–n–p width ratio. The lowest specific on-resistance occurs at a LDMOS gate width 6× wider than the p–n–p width.

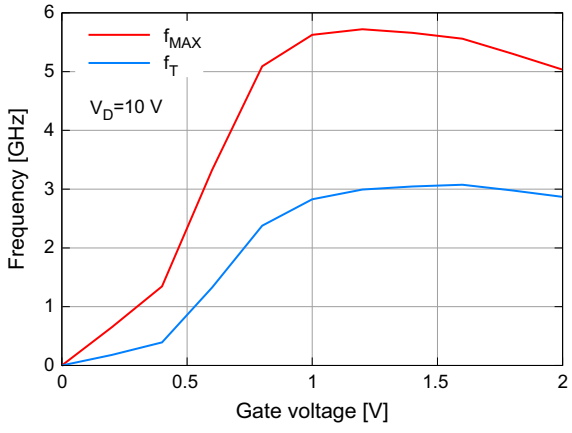

Fig. 13. The measured cut-off frequencies for an anode voltage of 10 V.

increase again. That is shown in Fig. 12 where the specific on-resistance for the LIGBT is plotted for four different LDMOS to p–n–p width ratios. From the figure, the optimum ratio seems to occur at a LDMOS width 6× wider than the p–n–p width. At that point the specific on-resistance is around 185 mΩ mm^2, which is a very low value; about 3–4 times lower than what has been reported for other 200 V LIGBTs on SOI [16].

S-parameter measurements were carried out with the NVA at different frequencies, using RF-probes and a separate DC-probe for the high-voltage buried n-layer. The DC-bias to the device was provided through internal bias-tees in the NVA. The parasitic contribution from the RF-pad pattern was de-embedded using open-pad structures and calibration standard procedures. From the S-parameters the current-gain cut-off frequency f_T and the unit power-gain cut-off frequency f_{MAX} were extracted at different bias conditions. Fig. 13 shows the f_T and f_{MAX} as a function of gate voltage for a LIGBT where the gate width of the LDMOS is 3× of the p–n–p device. The anode voltage is 10 V. The maximum f_T is 3 GHz and f_{MAX} is 5.6 GHz. Considering a breakdown voltage of 220–230 V these cut-off frequencies are among the highest reported for silicon devices in this range of breakdown voltage. The roll-off observed, is mainly due to the roll-off in transconductance observed in the LDMOS transistor and to some extent due to the non-linear gate capacitance.

Finally, off-state capacitances were extracted from the measured S-parameters at 1 GHz, see Fig. 14. The capacitive coupling

Please cite this article in press as: Olsson J et al. A new latch-free LIGBT on SOI with very high current density and low drive voltage. Solid State Electron (2015), http://dx.doi.org/10.1016/j.sse.2015.08.011

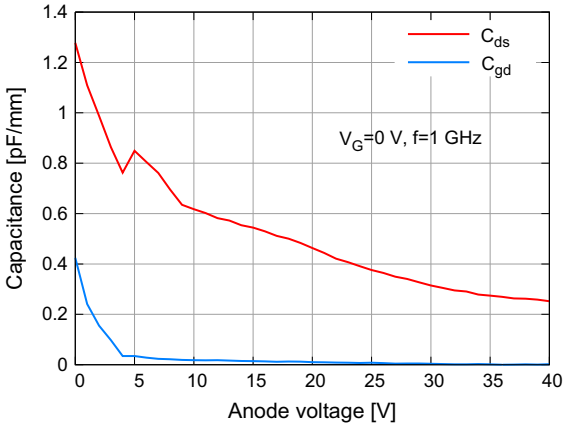

Fig. 14. The off-state anode-source capacitance (Cds) and the gate-anode (Cgd) capacitance extracted from S-parameters at 1 GHz.

between the anode and the gate (Cgd) is very low, as expected due to the separation of the LDMOS and the p–n–p device. The anode-to-ground (source and collector) capacitance is very low, in the order of 0.3 pF/mm for an almost fully depleted SJ-region. This indicates that switching performance and as well as RF-power performance can be expected to be very good. This is planned to be evaluated in the near future.

The results presented in this paper clearly demonstrate that the new LIGBT concept offers latch-free operation and astonishing performance. Furthermore, it is possible to use very low control voltage on the gate, enabled by the separation and the possibility to use a very wide LDMOS. The design of the p–n–p device is very critical; effective shielding of the base to prevent LDMOS breakdown, careful RESURF of the SJ-region and the anode/n-buffer region [16] to prevent premature off-state breakdown and optimize on-state voltage drop, V_{ON}.

4. Conclusions

A new LIGBT concept on SOI is demonstrated. By separation of the MOSFET part and the bipolar part of the device, parasitic latch-up is totally eliminated. The LIGBT is manufactured in a 1 μm BOX SOI foundry technology using a 12 V LDMOS transistor as the MOSFET part of the device. The demonstrated device has an off-state breakdown voltage higher than 200 V and extremely high current densities in excess of 3 A/mm (p–n–p width) with low drive voltages. The device offers unique opportunities to tune and optimize the device performance by separate scaling of the different device parts.

Acknowledgment

The authors would like to thank the GHz Centre at Chalmers, Gothenburg, Sweden, for performing the high-frequency NVA-measurements.

References

[1] Sambi M, Gallo M, Galbiati P. 190V N-channel lateral IGBT integration in SOI 0.35 μm BCD technology. In: Electron devices meeting, 2008. IEDM 2008. IEEE International; 2008. p. 1–4.
[2] Letavic T, Petruzzello J, Claes J, Eggenkamp P, Janssen E, Wal Avd, 650V SOI LIGBT for switch-mode power supply application. In: 18th ISPSD; 2006.
[3] Kho ECT, Hoelke AD, Pilkington SJ, Pal DK, Abidin WAWZ, Liang Yew N, et al. 200-V lateral superjunction LIGBT on partial SOI. Electron Device Letters, IEEE 2012;33:1291–3.
[4] Appels JA, Vaes HMJ. High voltage thin layer devices (RESURF devices). IEEE IEDM Tech Digest 1979:238–41.
[5] Tee E, Hölke A, Pilkington S, Pal D, Yew N, Abidin W. A review of techniques used in lateral insulated gate bipolar transistor (LIGBT). IOSR J Electr Electron Eng 2012;3:35–52.
[6] Park IY, Kim SH, Choi YI. Buried gate SOI LIGBT without latch-up susceptibility. In: SOI conference, 1998. In: Proceedings. 1998 IEEE International; 1998. p. 57–8.
[7] Disney DR, Plummer JD. SOI LIGBT devices with a dual P-well implant for improved latching characteristics. In: Power semiconductor devices and ICs, 1993. ISPSD '93. Proceedings of the 5th international symposium on; 1993. p. 254–8.
[8] Kang EG, Sung MY. A small sized lateral trench electrode IGBT for improving latch-up and breakdown characteristics. Solid-State Electron 2002;46 (2):295–300.
[9] Wensuo C, Gang X, Bo Z, Zehong L, Zhaoji L. Novel lateral IGBT with n-region controlled anode on SOI substrate. J Semiconductors 2009;30:114005-1–5-4.
[10] Choi W-B, Sung W-J, Park C-I, Kim S, Sung MY. New lateral insulated-gate bipolar transistor on silicon-on-insulator. J Korean Phys Soc 2002;40:645–8.
[11] Eklund KH. Semiconductor device wherein a first insulated gate field effect transistor is connected in series with a second field effect transistor. US8264015 B2; 2012.
[12] Vestling L, Olsson J, Eklund K-H. Drift region optimization of lateral RESURF devices. Solid-State Electron 2002;46:1177–84.
[13] Olsson J, Rorsman N, Vestling L, Fager C, Ankarcrona J, Zirath H, et al. 1 W/mm RF power density at 3.2 GHz for a dual-layer RESURF LDMOS transistor. IEEE Electron Dev Lett 2002;23:206–8.
[14] Kho Ching Tee E, Antoniou M, Udrea F, Hoelke A, Ng LY, Bin Wan Zainal Abidin WA, et al. Analysis on the off-state design and characterization of LIGBTs in partial SOI technology. Solid-State Electron 2014;96:38–43.
[15] Olsson J. Self-heating effects in SOI bipolar transistors. Microelectron Eng 2001;56:339–52.
[16] Tee EKC, Antoniou M, Udrea F, Holke A, Pilkington SJ, Pal DK, et al. 200 V superjunction N-type lateral insulated-gate bipolar transistor with improved latch-up characteristics. Electron Devices, IEEE Trans 2013;60:1412–5.

Please cite this article in press as: Olsson J et al. A new latch-free LIGBT on SOI with very high current density and low drive voltage. Solid State Electron (2015), http://dx.doi.org/10.1016/j.sse.2015.08.011