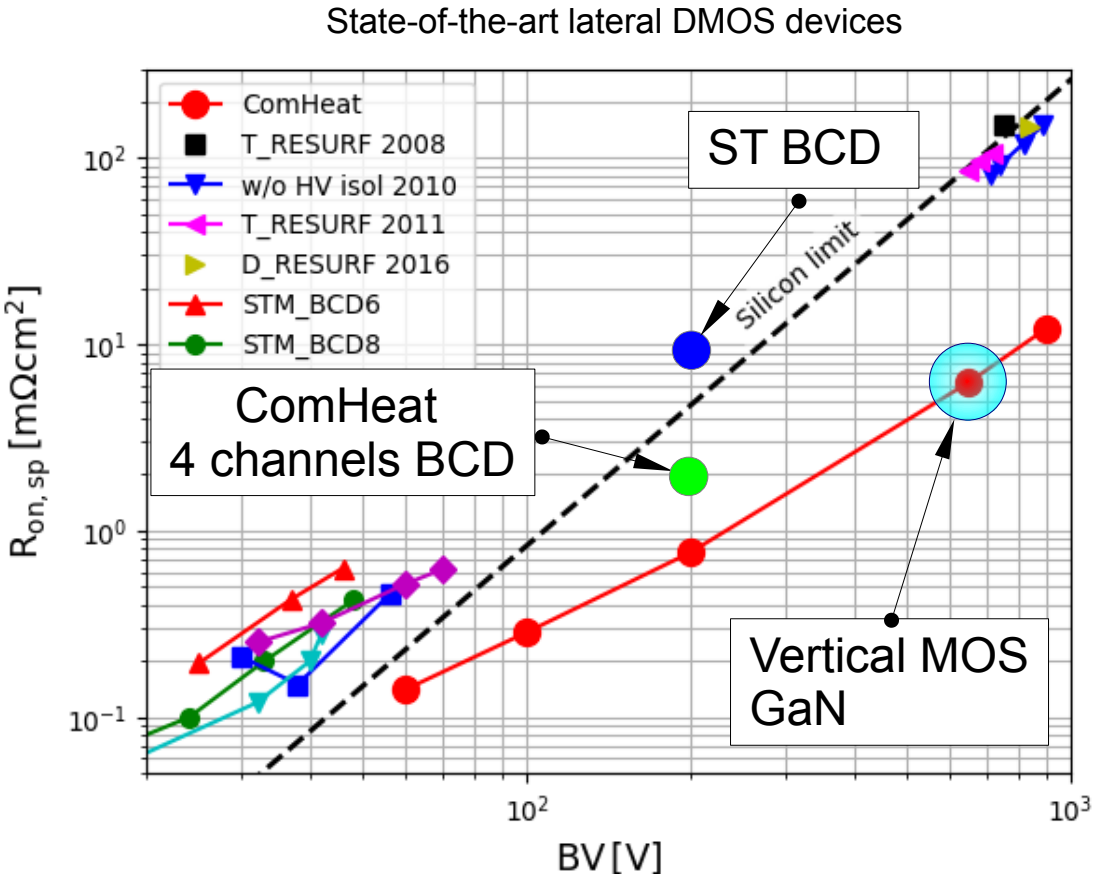
ComHeat Microwave

- Comheat Microwave founded 2005 with main strategy to develop new high voltage devices in combination with CMOS and to support the transfer of these devices into production.
- Dr. Klas-Håkan Eklund
  - Been in the industry for 50 years with main focus to develop high voltage devices in combination with CMOS.
  - Jointly founded (Key founder) NASDAQ listed USD 500m company
  - 20+ patents jointly or solely, related to Power Semiconductors.
- Dr. Lars Vestling
  - Thesis: Design and modeling of high-frequency LDMOS transistors.
  - Working 20 years in the industry mainly developing high-voltage silicon devices.

New LDMOS - Status of the design

- LDMOS device design ready to be implemented in silicon
- Concept is competitive for voltages from 60V up to 900V.
- Product specifications and SPICE-models available.



Capacitance

- Capacitance comparison with similar discrete Si-device (Infineon CoolMOS).
- Miller capacitance (Crss) much lower.

ME-LDMOS Power Transistor – 650V

ComHeat Microwave

November 23, 2020

1 Electrical characteristics

T_j=25 °C unless otherwise specified

1.1 Maximum ratings

Parameter	Symbol	Value	Unit	Test conditions
Gate voltage	V_G	±5	V	
MOSFET dv/dt ruggedness	dv/dt	50	V/ns	

1.2 Static characteristics

Parameter	Symbol	Value	Unit	Test conditions
On-resistance	$R_{DS(on)}$	1.2	Ω	V_G=5 V, I_D=1 A, T_j=25 °C
		2.0		V_G=5 V, I_D=1 A, T_j=125 °C
Drain current	$I_{D(sat)}$	3.2	A	V_D=20 V, V_G=5 V, see fig. 1
Zero gate voltage drain current	I_{DSS}	<1	µA	V_D=600 V, V_G=0 V, T_j=25 °C
		<100		V_D=600 V, V_G=0 V, T_j=125 °C
Threshold voltage	$V_{GS(th)}$	0.46	V	V_{GS}=V_{DS}, I_D=1 mA, T_j=25 °C
		0.46		V_{GS}=V_{DS}, I_D=1 mA, T_j=125 °C
Breakdown voltage	$V_{br(off)}$	>650	V	V_G=0 V
Pinch voltage	V_P	6.5	V	V_G=0 V

1.3 Dynamic characteristics

Parameter	Symbol	Value	Unit	Test conditions
Input capacitance	C_{iss}	73	pF	
Output capacitance	C_{oss}	4.2	pF	V_G=0 V, V_D=100 V, 1 MHz, see fig. 2-3
Reverse transfer capacitance	C_{rss}	0.001	pF	
Equivalent output capacitance (energy related)	$C_{o(er)}$	3.3	pF	V_G=0 V, V_D=0 V to 480 V
Equivalent output capacitance (time related)	$C_{o(tr)}$	37	pF	V_G=0 V, V_D=0 V to 480 V
Switching times for resistive load				
Turn-on delay time	$T_{d(on)}$	0.15	ns	
Rise time	T_{rise}	3.1	ns	V_{DD}=300 V, V_G=5 V,
Turn-off delay time	$T_{d(off)}$	4.2	ns	R_L=150 Ω
Fall time	T_{fall}	3.7	ns	
Switching times for inductive load				
Turn-on delay time	$T_{d(on)}$	0.15	ns	
Rise time	T_{rise}	1.1	ns	V_{DD}=300 V, V_G=5 V,
Turn-off delay time	$T_{d(off)}$	11	ns	I_D=1.0 A
Fall time	T_{fall}	2.8	ns	

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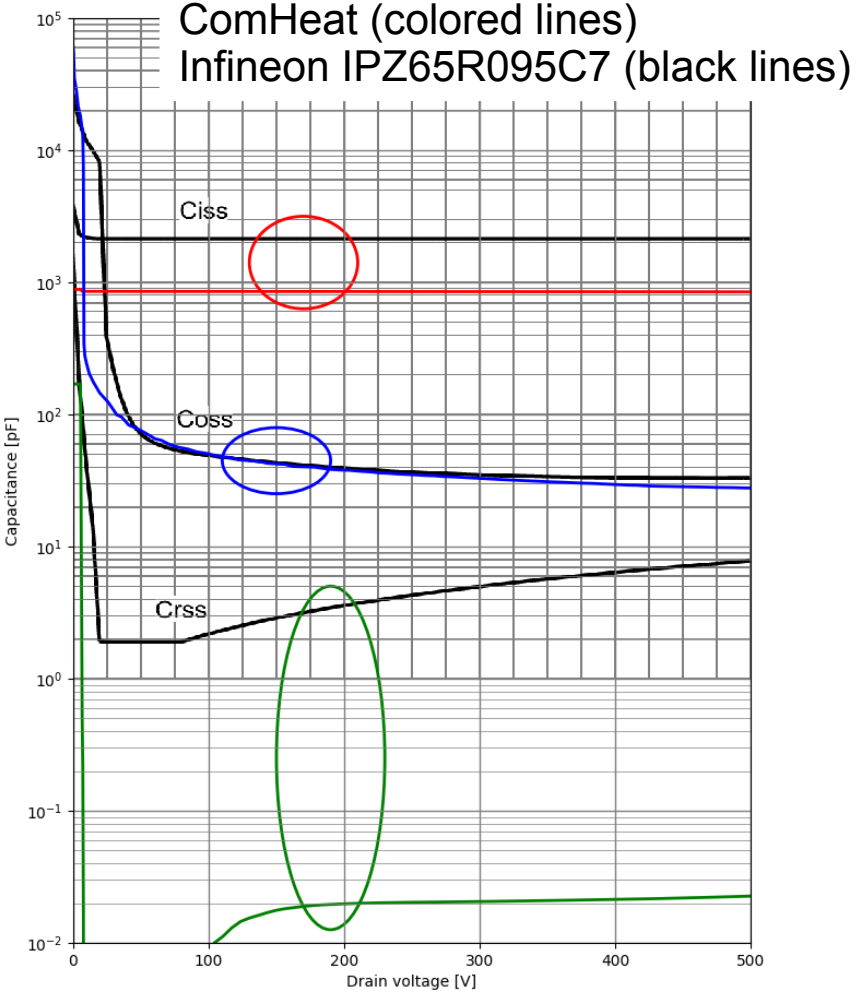


Electrical data comparison – 650V

	ComHeat 650V (LDMOS)	Si SJ (vertical) IPZ65R095C7	SiC (vertical) C3M0060065D	GaN (lateral) GS66504B
$R_{DS,on}$	100mΩ	100mΩ	100mΩ	100mΩ
$V_{GS(Th)}$	0.5V	3.5V	2.3V	1.7V
C_{iss}	730pF	2000pF	600pF	120pF
C_{oss}	42pF	31pF	90pF	80pF
C_{rss}	0.01pF	2pF	9pF	0.8pF
Q_g	7nC	48nC	28nC	3nC

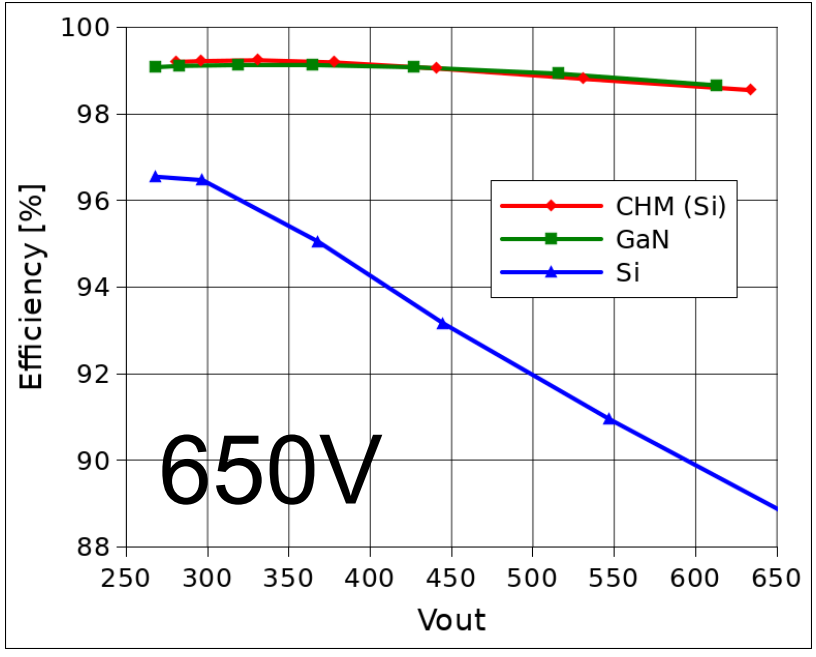
All devices normalized to 100mΩ, capacitances at V_G=0V, V_D=100V

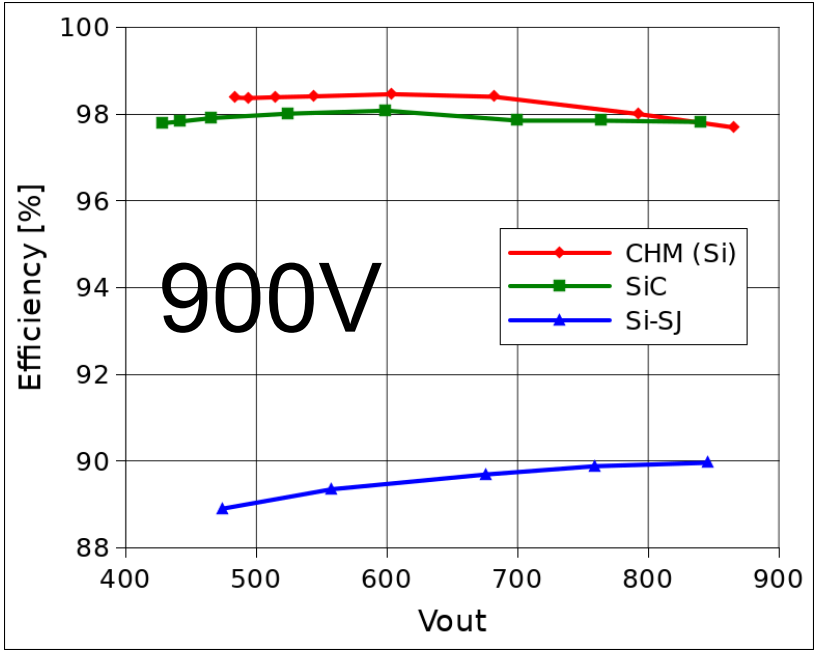
Electrical data comparison – 200V

	ComHeat 200V	Si-LDMOS NXP MRFX1K80H
$R_{DS,on}$	80mΩ	80mΩ
$V_{(BR)DS}$	230V	193V
$V_{GS(Th)}$	0.5V	2.5V
C_{iss}	380pF	760pF
C_{oss}	25pF	203pF
C_{rss}	0.04pF	2.9pF

Comparison with GaN (650V) and SiC (900V)

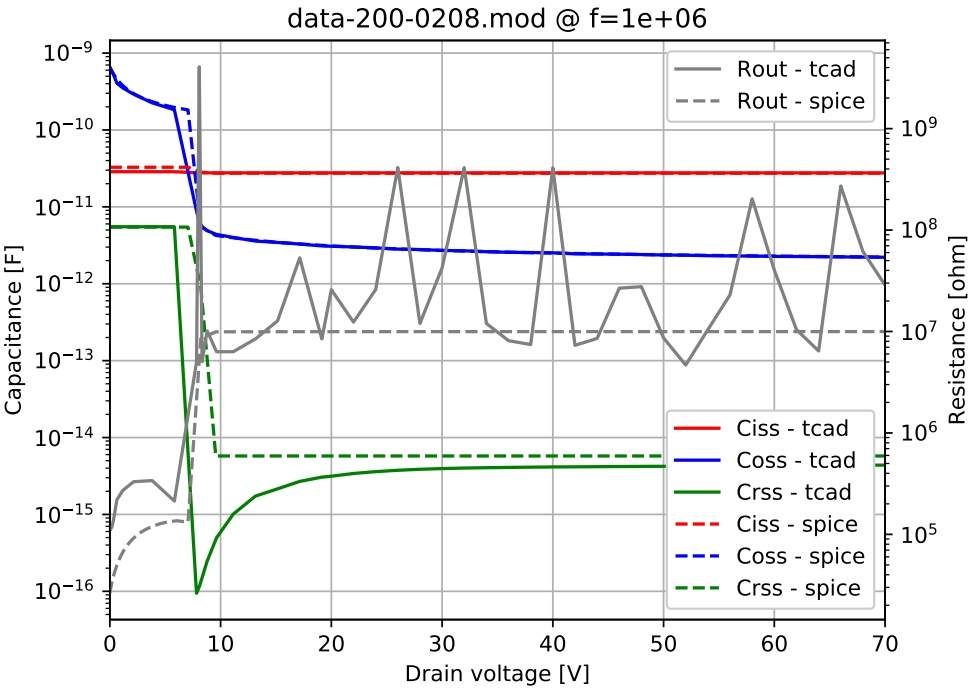
- Boost converter, 1 MHz
- Vin = 250V and 400V
- SPICE-simulation





SPICE model

- A compact model is developed and implemented in SPICE.
- Model parameters extracted from TCAD data.
- Plot shows comparison between TCAD (solid) and model (dashed).



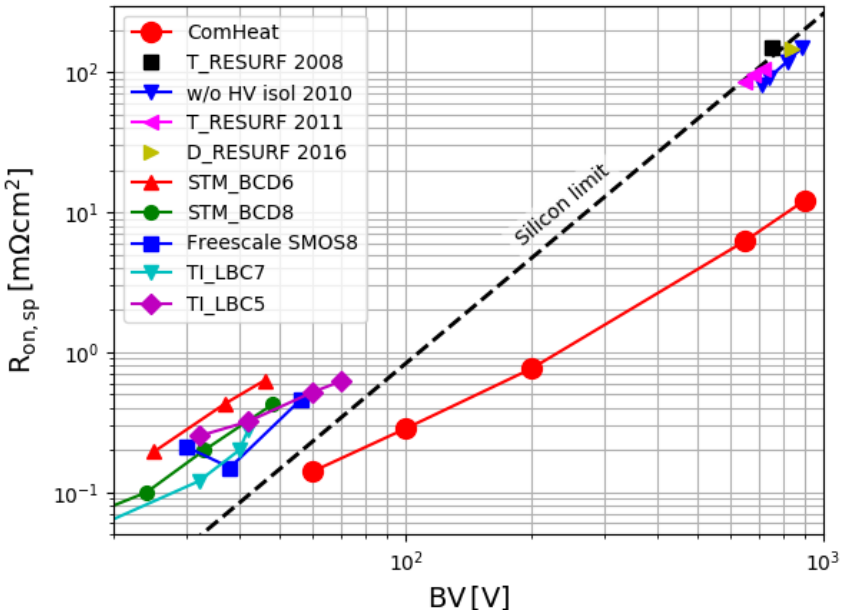
SPICE (dashed) - TCAD (solid)

Manufacturing requirements

- New LDMOS preliminary based on Silicon using strandard available equipment and processes used in semiconductor industry.

Device costs

- Die size reduction by a factor 5 and higher yield means lower manufacturing cost and less expensive packaging.

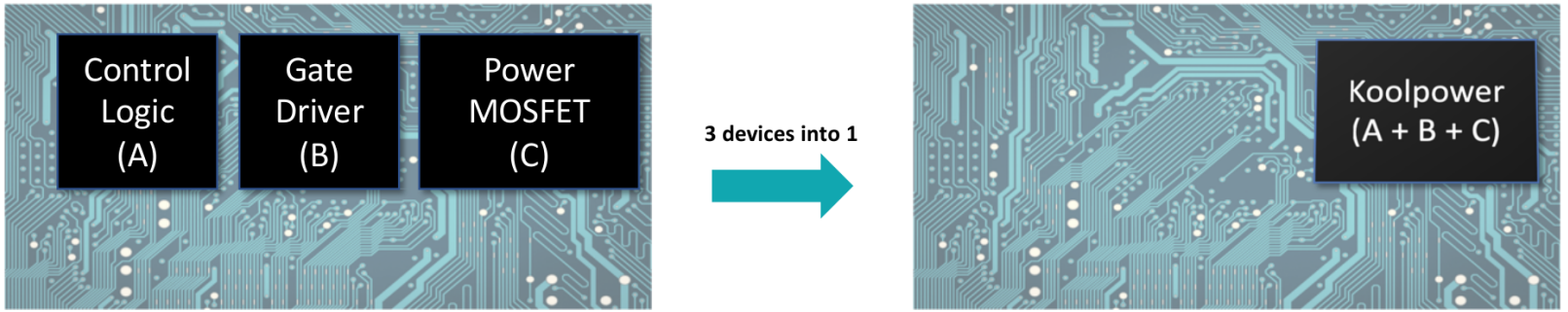


Functionality benefits

- Key capacitances will reduce with die size but especially the Miller capacitance has been further reduced to 1-10% which reduces power consumption, switching times but also increases reliability and robutness.
- Gate charge can be designed to be very low, partly due to lower gate voltages. Low gate charge is very important for efficient switching and simplifies gate drive design.

System Integration

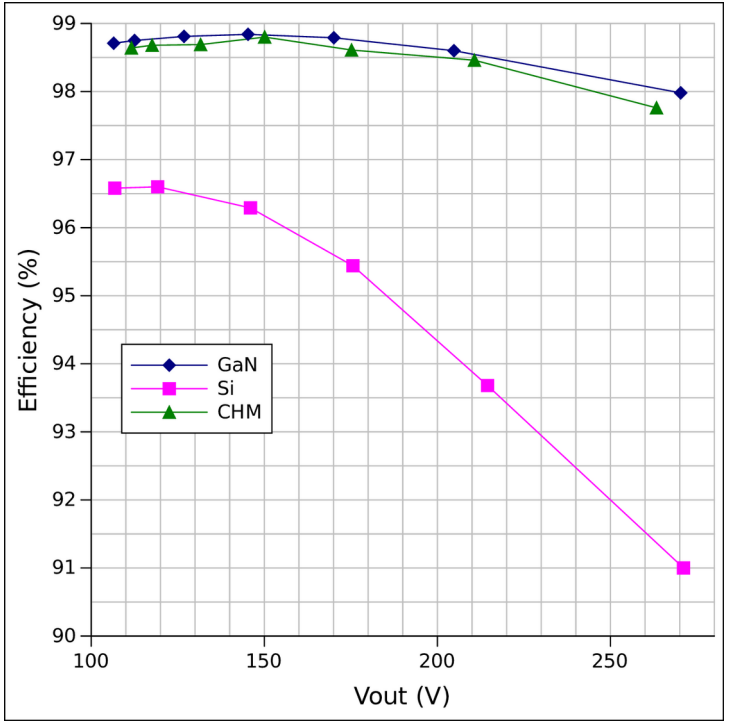
- Compability with CMOS even down to state-of-the-art with 1.8V gate drive logic and system integration on-chip.
- The device can be driven directly from CMOS. No need for an additional power supply.
- Actually, the concept can replace 3 devices with 1 device
  - discrete power device, gate driver and CMOS logic



GaN efficiencies at Silicon cost

- Comparison of GaN and ComHeat-LDMOS (650V).
- Switched boost converter at 1 MHz and V_{in}=100V.

- LDMOS size about the same as GaN.
- LDMOS cost less than half of GaN.
- We get GaN efficiencies at Silicon manufacturing cost



Switched boost converter

- Comparison with GaN-device and standard Si-device in a boost converter configuration.
- 650V-devices in a SPICE-simulation comparison.
- Switch frequency 1 MHz and V_{in}=100V.

- Switch device inside red square.
- Ideal circuit elements outside red square.